

## REMARKS/ARGUMENTS

This paper responds to the Office Action of June 17, 2004. Applicant respectfully requests reconsideration of the application. A Petition for Extension of Time extends the period for response through October 18, 2004.

Claims 1-71 are now pending, a total of 71 claims. Claims 1, 2, 8, 21, 25, 35, 38, 46 49, 59 and 61 are independent. Of these, claims 1, 35 and 38 are allowed.

The amendments to the claims, to change “first” to “an earlier ... and before a later,” are intended to broaden the claims, to eliminate any question that the claim only applies to the first of several side-effects of an instruction.

### I. Claims 2 and 8

Claims 2 and 8 are discussed in paragraph 4 of the Office Action. Claim 2 recites as follows:

2. A method, comprising the steps of:

decoding and executing instructions of a complex instruction set of a computer, the instruction set having variable-length instructions and many instructions having multiple side-effects;

storing information describing the decoding of the complex instructions into architecturally-visible processor registers of the computer.

The Office Action merely states that the second paragraph of this claim corresponds in some unspecified way to two lengthy portions of Phillips '074, col. 3, line 57 to col. 5, line 54, and col. 11, lines 30-65. However, the Office Action does not indicate which of the host of things discussed in these portions of Phillips '074 corresponds to the “decoding,” which to the “processor registers,” or how any “processor register” might be “architecturally-visible.” “When a reference is complex ... the particular part relied on must be designated as nearly as practicable. The pertinence ... must be explained.” 37 C.F.R. § 1.104(c)(2). The Office Action simply points to some 150 lines of text describing a multitude of elements, without indicating which are thought pertinent, or how.

Because of these omissions from the Office Action, Applicant can only guess at the Examiner’s view. Without waiving the opportunity to reply to a proper rejection, and in an effort

to advance prosecution, Applicant notes that the DIP, TIP, and NIP of col. 4, lines 24-26 of Phillips '074 are not “architecturally-visible” – Philips '074 discusses no way for software to detect the value of the DIP, TIP and NIP. The DIP, TIP and NIP are hardware implementation structures that are deliberately kept below architectural visibility.

Because the Office Action is incomplete, no rejection is raised. Further, to the extent that Applicant can surmise the Examiner's view, there appears to be no correspondence between the indicated portions of Phillips '074 and claim 2. Claim 2 may be allowed. Applicant respectfully requests notice of same.

Claim 8 recites similar limitations and is likewise neither rejected nor rejectable over Phillips '074.

## **II. Claims 21 and 25**

The Office Action states that Philips '074 and Cheng '804 are thought relevant to claim 21; however, the Office Action does not offer an explanation of this relevance on an element-by-element basis. Claim 21 recites as follows:

21. A method, comprising the steps of:

executing a program in user state of a computer, the program coded in an instruction set having many instructions with multiple side-effects and the potential to raise multiple exceptions;

in response to recognizing an exception occurring in an instruction after an earlier side-effect of the instruction has been architecturally committed and before a later side-effect of the instruction is architecturally committed, transferring control to a software exception handler for the exception, and resuming execution of the excepted instruction after completion of the exception handler, processor registers of the computer being designed to architecturally expose sufficient information about the intermediate state of the excepted instruction that the transfer and resume are effected without saving intermediate results of the excepted instruction on a memory stack.

The limitations “user state of a computer,” “an exception occurring in an instruction after an earlier [or “a first”] side-effect of the instruction has been architecturally committed,” and “the intermediate state of the excepted instruction” appear to be omitted from the Office Action.

The pertinence of Cheng '804, col. 2, line 50 to col. 3, line 9 is not apparent. Paragraph 15 of the Office Action asserts that the various combinations of 23 claims are all “taught” in one

30-line section of Cheng '804. Of those 23 claims, only one is even mentioned in paragraph 15. In the event of any future rejection, Applicant requests a meaningful statement of grounds, as required by 37 C.F.R. § 1.104(c).

Where claim 21 is directed to “the intermediate state of the excepted instruction,” Cheng '804 is directed to interrupts that occur at instruction boundaries. Cheng '804, col. 2, lines 4-6, states “After the interrupt has been serviced, execution continues with the next instruction...” Unless Cheng is only concerned with exceptions at instruction boundaries, continuing with the “next instruction” without completing the “excepted instruction” would often lead to incorrect results.

Because the Office Action does not address all claim limitations, no rejection has been raised. Similarly, because the Office Action makes no showing of “reasonable expectation of success,” as required by MPEP § 2143.02, no obviousness rejection is raised. Further, the claim recites at least one limitation that is absent from the indicated portions of the references. Claim 21 may be allowed.

Claim 25 recites similar limitations and is likewise neither rejected nor rejectable over Phillips '074 and Cheng '804

### **III. Claims 46 and 49**

Paragraph 12 of the Office Action mentions claim 46 in summary fashion, but the Office Action nowhere considers the limitations of claim 46 on an element-by-element basis. No rejection exists. Claim 46 recites as follows (emphasis added):

46. A method, comprising the steps of:

while executing a program coded in an instruction set exposed for execution by programs stored in a main memory of the computer, recognizing an exception occurring in a program, and in response, architecturally exposing in processor registers of the computer information describing a processor state of the computer and transferring execution to an exception handler;

after completion of the software exception handler, resuming execution of the excepted program based on the information in the processor registers;

the processor registers and general purpose registers of the computer architecturally exposing sufficient processor state and providing sufficient working storage for execution of the exception handler and resumption of the program, without storing processor state to the main memory.

Because the Office Action does not designate “the part relied on,” let alone explain the “pertinence,” of Phillips ’074 or Cheng ’804, the Office Action fails to meet the requirements of 37 C.F.R. § 1.104(c)(2), and Applicant is unable to respond directly. If any rejection is raised in a future Office Action, Applicant requests an element-by-element showing of the pertinence of the prior art to the claim, with particular attention to the portions underlined above.

Claim 49 recites similar limitations, and is likewise not rejected.

#### **IV. Claims 59 and 61**

Paragraph 12 of the Office Action mentions claim 59 in summary fashion, but no paragraph of the Office Action considers the limitations of claim 59 on an element-by-element basis. Claim 59 recites as follows:

59. A method, comprising the steps of:  
fetching instructions in a first external instruction set from a memory, and,  
for at least some instructions of the first instruction set, issuing two or more  
instructions in a second form into an execution pipeline;  
architecturally exposing an intra-instruction program counter value when  
an instruction of the first instruction set raises an exception at an intermediate  
point.

The Office Action makes no reference to the “intra-instruction program counter” recited in claim 59. No rejection exists.

Claim 61 also recites an “intra-instruction program counter” and is likewise not rejected.

#### **V. Dependent claims**

A number of dependent claims that are supposedly “rejected” recite limitations that are not addressed in the Office Action. Such piecemeal examination is discouraged by 37 C.F.R. § 1.105 and MPEP § 707.07(g). It is requested that any future Office Action indicate the allowability of any claim that recites a limitation against which no prior art is cited.

Applicant also draws the Examiner’s attention to MPEP § 2143.03, that requires that every element be taught or suggested in the prior art before a claim can be rejected. Paragraphs 11 and 15 of the Office Action concede that certain claim limitations are totally absent from the prior art relied on. After that concession, the law provides for no “however” that can support a

rejection. Applicant requests that any future Office Action cite particular prior art against each limitation of each claim that may be rejected.

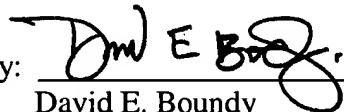
Dependent claims 3, 5, 10, 11, 13-20, 23, 24, 26, 28-34, 46-48, 50-52, 54, 56-58, 62-65 and 67-71 are patentable with the independent claims discussed above. In addition, the dependent claims recite additional features that further distinguish the art.

In view of the amendments and remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. Particularly in light of Applicant's inability to address the Examiner's view because of a lack of explanation of that view, Applicant urges the Examiner to phone Applicant's undersigned counsel at the number noted below. A Petition for Extension of Time for extends time for one month. In the event that further extension of time is required, Applicant petitions for that extension of time required to make this response timely. Kindly charge any additional fee, or credit any surplus, to Deposit Account No. 23-2405, Order No. 114596-27-0052BS.

Respectfully submitted,

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